OCR Computing H446: Component 3

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# Section 1: Analysis

All solutions begin with an adequate analysis of the problem. This sets a framework for the solution to be built within, with clear expectations. This helps prevent resource consuming ‘feature creep’ that can lead to missed deadlines and the eventual derailment of a project. The analysis will begin by focusing on the problem itself, before considering the stakeholders and other solutions to the problem. Finally, a rigid specification will be set for the solution.

## Problem Identification

The chosen problem is that of simulating a computer processor and operation for the purposes of teaching computer science. The software should be appropriate for a variety of educational institutions and be considered on par or above the quality level of competing software. The problem is almost exclusively solvable using computational methods, and is amenable to being solved in this way for the following reasons:

### Complexity of the Simulation

A computer processor involves many complicated aspects and this makes it ideal for simulation as a piece of software. Working through a simulation by hand would be incredibly time consuming especially when considering the great speed at which modern processors operate. To simulate even a second of a modern processor would take years, if not decades. By simulating the processor using a modern computer, often capable of running at speeds beyond a hundred million operations a second, we are able to run it at speeds that will allow the user to test basic programs.

### Educational Requirement

The idea of the program is for it to be used to help teach and give people an understanding of a processor. It would be impossible for somebody to manually simulate a processor without having the prerequisite knowledge. By making it an interactive simulation, students will be able to try different things and visualize the various cycles within a processor. Processors can seem to be quite an abstract idea, so being able to interact with a simplification will enable people to grasp a deeper understanding.

### Controlled Environment

A processor is a relatively simple model and can be considered a closed environment. This is the opposite of more complicated systems such as weather and chemical reactions that are often subject to external influencing factors that are difficult to take account for. A tiny inaccuracy in a weather forecast will simply be compounded as the simulation runs. Because a processor is simple, and a closed environment, the simulation will remain accurate, making it an ideal thing to simulate using a computer.

### Ease of Visualization

A modern computer is equipped with graphics capabilities and this means it is possible to render images that will accurately represent the model. This graphics would simply and clearly explain the workings of a processor. This will also make the learning more engaging, as many people tend to be more interested by a visual explanation than a verbal one.

### Existing Infrastructure

Almost all computer science lessons are taught in classrooms with access to computers, which makes this problem incredibly amenable to being solved using a computational solution. This means the software will be able to be conveniently accessed by its key users, and that the staff will not have to book the room in order to use the software. Students may be able to use the software at home to expand their own understanding and revise.

## Stakeholders

Stakeholders remain one of the most important considerations in the development of software. Ultimately, if the software is not appropriate for its stakeholders then the project is a failure. It is important to note that, in many cases, it is impossible to please all stakeholders involved in a project, as many often hold conflicting requirements.

I have decided to primarily target educational institutions because the requirements of a technical professional will contrast too greatly with those of a student. Complexity of the processor must be abstracted to an understandable level, but by doing this valuable information to a professional is lost. Simulating a modern x86 processor is also beyond the scope of my own personal understanding, as the instruction set has grown significantly more complicated from its conception.

### School Management

The bureaucratic element of many organizations is easily ignored when it comes to the production of software, as they will not be final end-users of the software. However, software must still meet many requirements produced by the management of any organization in order for it to be adopted.

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| User Requirements | Justification |
| Affordable | Software must be deemed economically viable for an organization to adopt it. This does not only cover the cost of purchasing software, but also support agreements and the time as well as financial cost of training the users. |
| Secure | Software must not present an additional risk to the system, intentionally or unintentionally. Vulnerabilities continue to be misused in software in order to gain a foot hold or escalate an attack, and it is the responsibility of the software developer to ensure this is not possible. This is not overly applicable to my solution because the software will not interact with any networks, and hence not present an attack vector. As my solution will be written in a high level language, it is unlikely the software will be vulnerable to memory attacks used for privilege escalation. |
| Compatible | Software will be more convenient for adoption by an organization if it is compatible with existing systems, both technically and bureaucratically. Software must be adapted to integrate with any hierarchies or procedures that are ingrained within an organization, as this means that integration will be a simpler, and cheaper, process. For our solution, this means the application should be of adequate depth to easily meet the teaching requirements of common Computer Science |

### Teaching Staff

Teachers represent the first of the user groups. The software must be apt to their needs, as they will spend the most time interacting with the software as it is used year on year with different classes. Software that does not adequately fulfil their requirements will become disused, with more appropriate solutions being found.

Mr. Albanozzo is a computer science teacher at Bournemouth School. He first suggested the project because he was frustrated with the limitations proposed by the Little Man Computer currently used to teach about processors and felt that a better version could be made.

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| User Requirements | Justification |
| Simplicity and Demonstrability | Software must be simple to use and demonstrate. Software that is self-explanatory is easier to teach the use of, and reduces questions raised by students, allowing more time to teach the course content. Demonstrable software ensures that the UI is clearly visible and clear when shown on a projector and that actions are easily reproducible. |
| Accurate | The software must accurately represent the content of most computer science courses. If the software is misleading it may cause a lack of understanding of the course, which may be complicated to fix. On the other hand, if the software is accurate, it will further their knowledge and allow them to gain a deeper understanding of computer processor architecture. |
| Fast and Stable | The software must be responsive, load quickly, and not experience crashes or data corruption. Slow software holds up the learning process and crashes lead to the loss of work, both of which may require the intervention of the teaching staff to resolve, wasting valuable time. |

### Students

Students act as the primary target for the use of the software. They mostly share requirements with teaching staff, including the requirements for software to be fast and stable, for it to be compatible with their course, and for it to be simple enough to be quickly grasped. There are a few unique requirements.

Emilio is a run-of-the-mill computer science student at Bournemouth School. Whilst he performs well in most areas of the course, he struggles most with processors and assembly. He feels that Little Man Computer does not currently make many concepts needed at A-Level clear. He thinks he would be more easily able to understand the concepts if he had something to visualize how the data moved around the processor.

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| User Requirements | Justification |
| Adaptable | Students have a varied range of abilities, the software should be able to offer multiple levels of difficulty to continue to keep stronger students engaged. Many pieces of software aimed at educational institutions fail to cater for all levels of student, and either are seen as too complex by weaker students and too simple by stronger students. |
| Clear | The student must be able to clearly see how data and instructions are moved around the system and how the important registers interact with each other. This will enable them to get a better understanding and help them to more easily remember the concepts as they can see them visualized. |

## Existing Solutions

Existing solutions provide great inspiration as to the required features of an application if it is to compete within the same market. Weaknesses of existing applications can be used to bolster your own and to improve the user experience significantly. However, it should be noted that not all pre-existing solutions may seek to solve the problem in the same way, with some focusing on alternative user groups

### ArmSim

ArmSim is a realistic simulation of an ARM RISC processor designed for testing assembly code designed for ARM processors before it is used on physical hardware. It provides a rather gray UI and provides a simple way for a programmer to view the running memory of the simulated processor. The UI is not particularly intuitive and the software is mainly aimed at professional programmers who will quickly become accustomed to their tools.



ArmSim does not provide an interface for writing code and instead allows a programmer to use an existing IDE they own to write the assembly and compile it to machine code before importing it. This is far more suitable for a professional who will already have an established workflow with their software and may have to use a certain IDE because of rules set by their management. It acts purely as a simulation of the processor, rather than trying to also act as an IDE.

It provides access to all of the registers that are found within an ARM processor as well as providing the ability to browse through the entire memory space, with a quick jump to an address feature. The stack is also provided as a separate sidebar to allow its contents to be better visualized compared to just browsing the memory locations. It provides the ability to step into and step through a program, or to run it as fast as the processor can. Data can be shown in the registers in decimal, hexadecimal or binary, depending on how comfortable the user is with each form.



The registers are demonstrated on the left side, with modified registers shown in red to clarify what has changed to the developer.

The simulation provides a one to one in-depth replica of an Arm processor, with the entire instruction set implemented with a fine level of detail. Software can be directly compiled to this instruction set from various language and can then be ran step by step through ArmSim. Whilst this level of detail and accuracy is essential to a seasoned programmer, it is unnecessary and perplexing for a student. Instruction sets and processors are far more complicated than the abstraction used by A-Level courses and ArmSim is likely to further confuse rather than help students.

ArmSim is provided as a compiled executable file. It is natively designed to run on Windows x86 64 or 32bit processors and the source code is not open. There has been some documented success at running it using the WINE (WINE Is Not an Emulator) platform on GNU/Linux and MacOSX.

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| Feature | Justification |
| Fast simulation | ArmSim’s ability to simulate an ARM processor at close to real speeds is useful for developers wanting to test their programs properly. It allows more complex algorithms to be designed. |
| Simple access to memory | ArmSim provides an easy way to browse the memory and this is useful for students and developers trying to understand their program and debug any issues with their algorithms as they can see the changes to the memory clearly. |
| Detailed Simulation | ArmSim provides a comprehensively detailed simulation of an ARM processor. A balance will have to be struck between simplicity and complexity for my simulation as it will primarily aimed at as a teaching tool. |
| Display of values in multiple bases | ArmSim provides the user the ability to view values in decimal, hex and binary and this is beneficial as it will allow users to familiarize themselves with the common bases used within the CompSci world. This is also beneficial as some values only make sense in certain bases (i.e Instructions are clearer in binary where you can see the divide between Opcode and Operand) |
| Console window to provide feedback | The console window acts a simple way for the program to inform the developer of issues, as well as providing the output of the processor to the user. It is less intrusive than pop-up messages and can be scrolled back through to view historical changes. |

### Little Man Computer

Little Man Computer (LMC) is a CPU simulation designed for teaching about assembly and the workings of a processor. It can run within the browser and provides a graphical interface for interaction. Unlike ArmSim it provides a basic editing interface where a simplified assembly instruction set can be written and then compiled into machine code.

LMC provides a variety of features such as the ability to change the simulation speed. This is useful for people wanting to see more about the workings of a processor since they can slow it down and see it step through each part of the Fetch Decode Execute (FDE) cycle. Others may want to speed it up so they can see their code that they have written running more fluidly. There is quite a low limit to this speed and it can be frustrating when you have written a more complicated algorithm (for example to calculate prime numbers) and it takes a long time to execute.

The LMC provides an incredibly simplified model, with only a few core registers such as the PC, IR and MAR. The memory itself has only 99 addresses and each of these is restricted to an integer from 0 to 999. The instruction set is cut down to a few basic instructions and there is only a single memory addressing mode that the user is not even made aware of.



LMC further abstracts the processor by showing all numbers and commands as base ten integers rather than showing them as their binary equivalents. This may make it easier for a newer student to understand, as at first binary instructions may seem intimidating; however this does obscure the fact that an instruction stored in memory is composed of two distinct parts, the operator and operand.

Whilst LMC does simulate only a handful of registers, they are all clearly shown within their own part of the UI. This makes it simple to see how the values of the registers change as the FDE cycle completes, something that you may be examined on at GCSE and A-Level.

The fact that LMC can be embedded within the browser has advantages as well as limitations. One of the prime advantages is portability. Browsers act as a layer of compatibility and this means that LMC can run across different operating systems as well as processor instruction sets. This also means that the application does not need to be pre-installed, only a relatively modern browser is needed, and for the most part this is already present in most schools. The biggest limitation of this is processing speed. Modern browsers and the JavaScript engine add lots of overhead to execution and this restricts how fast it is able to simulate the processor. JavaScript is also a problematic platform considering its varied implementation across not only versions of browsers, but browsers themselves. This makes it hard to predict how it will behave when deployed across a wider user-base.

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| Feature | Justification |
| Appealing Interface | An appealing interface makes the program more attractive to those learning to program, whilst seasoned developers are more used to more plain design. An appealing interface will also be easy to work with and not frustrate users. |
| Ability to adjust speed | The ability to adjust speed is useful for almost all users, as at lower speeds it is similar to step-through debugging. At higher speeds, the user can examine the overall effectiveness of the algorithm, especially more complicated ones. |
| Simplicity | LMC simplifies the architecture of a processor to a point where it is understandable, however my program must go further in ensuring that it also provides enough depth, which LMC does not. |
| Simple Assembly Editor | LMC provides a useful interface for writing the assembly, unlike ArmSim, and this allows the user to quickly make changes and retranslate the code rather than having to switch out to another application and reload the code. This editor could be taken further to help the user. |
| Values of registers clearly displayed | The values of each register, and how they connect to each other, are clearly displayed (for example the accumulator is show connected to the ALU) and this helps users get a better understanding of how a processor works. |

### Assembly Training Program (ATP)

Assembly Training Program is an old windows application designed to teach assembly at higher levels. The application does not run on newer versions of Windows, however it comes with comprehensive documentation that outlines the specifics of the simulated processor and I will instead examine this.

The ATP processor is known as the BEP/16 which is a hypothetical 16 bit processor based roughly on the popular Intel 8086 microprocessor platform, the processor from which the x86 instruction set still in use today derives from. This makes it still an accurate representation of how a modern processor works, as even though major changes have been made over the years, the base instruction set has remained primarily the same.

The BEP/16 provides 10 general purpose registers as well as a full 16 bit Program Counter, Stack Pointer, Flag Register and Overflow register. The 16 bit nature of the Program Counter limits the total RAM size to at most 64K addressable bytes, however the processor also offers another 16K bytes of stack, both of which are accessed in 2 byte words. This configuration is incredibly flexible, with the general purpose registers allowing more complicated programs to be written by students. The amount of RAM is more than enough for the purposes of most students.

The flag register provides multiple useful flags. This includes the carry bit, zero flag, sign flag as well as an overflow flag. Each flag takes up a single bit of space and are updated as calculations are carried out to reflect the current state of the processor. For example, the zero flag will be set if the result of an operation in the ALU is 0, and be reset back to false if another operation takes place that produces a different result.

The 16 bit nature of the processor provides more than enough resources (65,535 integer values) for most calculations, with some arguing that it could be enough to actually overcomplicate matters. However, the next natural step down would be an 8 bit processor, which would be incredibly restrictive in only being able to hand unsigned integers of 0-255. A 32 bit processor would be greatly in excess of the requirements of the users and introduce new challenges in terms of the UI, as more data would have to be displayed.

The instructions are provided in the typical MODE-OPERATION-OPERAND format, with 2 bits for the memory mode, 6 bits for the operation (providing up to 64 possible operations), 4 and 4 bits for selecting the registers used in the operations with the remaining 8 bits used for the operand. This format is more complicated than that used in the Little Man Computer but provides much more flexibility to the programmer, certainly making it more appropriate for universities and sixth-forms as opposed to GCSE level.

Unlike the Little Man Computer, ATP provides access to a variety of addressing modes. This is useful as at A-Level addressing modes are taught as part of the specification, yet are missing from a common teaching tool. The BEP/16 offers 7 addressing modes, with not all of these available for all instructions. Direct, Indexed and Indirect are exclusively reserved for the STR and LDR register-RAM transfer commands.

ATP also provides a rudimentary assembler with preprocessing features. This allows the user to write assembler rather than the direct machine code that is executed by the simulated processor. The assembler is little more than rudimentary, providing a few simple #DEF operations allowing constant values to be easily set and reused within the program. Registers may also be provided an alias. This seems like a useful feature, even for new programmers, as it will allow them to write code that is more self-explanatory and easily understood by others.

Software Interrupt Routines (SWI) are also provided by the BEP/16 infrastructure and act as a way for the programmer to interact with an user. Calling an SWI triggers a context switch, with all the registers being pushed onto the stack bar R0 which is used for communication between the program and the interrupt routine. Four software interrupts are provided: getInt, putInt, getChar, putChar. These are a particularly useful part of the simulation that could have just been abstracted, however instead they have been implemented properly and this means that the user can get an understanding of how the software interrupt process works, something that is required at A-Level.

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| Feature | Justification |
| Powerful instruction set | Allows the user to create more than just rudimentary programs and instead create more fully functioning programs. |
| Implementation of ISRs | Interrupt Service Routines are not defined in Little Man Computer but are required by the A-Level specification, the context-switching process could be clearly demonstrated. ISRs are also a useful way of the processor serving the requirement for input and output. |
| Appropriate Simplicity | Assembly Training Program strikes a careful balance in ensuring that the user is not overwhelmed with an entirely complete instruction set, instead only the core, most important, parts are implemented. |
| Multiple addressing modes | ATP provides multiple addressing modes to the user, something that is mentioned at A-Level, and this allows the user to write more efficient programs with, for example, indexed addressing. |
| Assembler with directives | The assembler within ATP supports useful directives for the developer. These speed up the programming process and allows constant values to easily be changed across the application. |

## Limitations

No project is without a scope and it is always important to have realistic expectations of what an application will be able to within the deadline and budget. The program will target the education market and I have drafted several relevant limitations to the project.

### Direct execution of compiled code

Whilst ArmSim provides the ability to run native code that has been compiled by GCC and other similar industry compilers, our application will not. There is limited use of this feature to students and it would require implementing the entirety of a comprehensive instruction set (e.g x86\_64 with 981 base instructions and 3683 variations of those [1] ), which is simply unrealistic within the deadline set.

### Ability to run on a wide variety of platforms

For my application I will most likely be using a .net based language and these executables do not natively run on operating systems other than Windows. Whilst it is possible to port them to compile with Mono (A .net alternative for GNU/Linux), this is simply not possible within the deadline set for the project.

### The entirety of an existing instruction set

Most of an existing instruction set will not be used by students day to day and to implement it within the timeframe set for the project would be unrealistic. Instead I will try to make my own instruction set in the style of x86 to allow people to get the gist of existing instruction sets

### Alternative architectures

My software will simulate a Von Neumann-esque processor. It would be too time consuming to implement multiple different architectures and would provide little advantage as students are not required to understand the exact workings of other architectures.

## Software and Hardware Requirements

It is reasonable to set out expectations for the kind of hardware and software required to be able to run my application. Choosing the frameworks and language to be used is often difficult, as no language is capable of dealing with all problems and choosing the wrong one can lead to more time being spent trying to work around a problem.

### Software

I have decided to choose C# with the .Net Framework as the language to use for my application development. Whilst it is not my favorite or most comfortable language, it is well suited to the problem for a variety of reasons:

#### Targeted Desktop Development

C# and the .Net Framework (Visual C#) was originally targeted at desktop development and provides a wide variety of useful classes for visual components (buttons, text boxes, panels etc) with a unified styling. This will allow me to produce a professional looking application quickly.

#### Fast

Once compiled C# is much faster than interpreted languages such as Python. This means it will be able to simulate more processor cycles each second, giving the user more flexibility. Of course it is not as fast as C++ and other lower level languages, but this is at the cost of usability when trying to rapidly prototype an application.

#### Type Safe

C# provides strict static typing as well as tight access control and this makes it an incredibly type safe language. This helps the developer, especially in larger projects, produce an overall more stable and predictable program that is not vulnerable to unexpected issues caused by dynamic types and casting. Stability is an incredibly important aspect of any commercial application, especially those where a user could lose work if the application crashes.

#### Comprehensive Tooling

Microsoft provides a comprehensive set of tools through its Visual Studio IDE that includes advanced debugging with stepping and watching, static code analysis and a WYSIWYG editor. This allows the application to be rapidly produced with easy results, which is important considering the short deadline on the project.

### Hardware

Hardware specification is something of a dark art as it can be hard to predict exactly how an application will perform until you have benchmarked it. However, rough guidelines can be drawn up from what we would expect from the average C# .Net application. Fortunately most schools provide computer science labs with higher specification machines so that they can run virtual machines etc and this provides us more room to work within.

Minimum requirements:

* Dual Core processor at 2.6 Ghz
* 4 Gigabytes of RAM
* Free disk space of 10GB
* Integrated graphics capability

Recommended requirements:

* Quad core processor at 3 Ghz
* 8 Gigabytes of RAM

## Features and Requirements

### Essential Features

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| Feature | Justification |
| Instruction set with enough depth for complex programs | My program must be able to allow students to challenge their own abilities by designing more complicated programs, software such as LMC simply does not have the depth required to allow students to stretch themselves adequately. |
| Simple and easily grasped user interface | The user interface must be quick to understand for new users. The interface should be accessible to a wide range of understandings and not confuse new users by presenting too much information. |
| The ability to modify the speed of the simulation | The user must be able to change the speed of the simulation in order to switch between wanting to understand the Fetch-Decode-Execute cycle on the microscopic level to wanting to write more complicated algorithms. |
| Accurate simulation of a processor according to the A-Level and GCSE specifications. | The processor should be designed to demonstrate the entirety of a processor according the A-Level specification with adequate depth to allow students to push themselves. There is no need for the processor to perfectly simulate an existing, more complicated, architecture. |
| A selection of example programs | Example programs for common algorithms should be included to demonstrate the abilities of the simulation as well as to help teach the user how to use the provided assembly. It would also be useful for users to learn how many of the core algorithms to Computer Science work. |
| Ability to save and restore the state of the processor | The user should be able to save the processor and the code currently stored in it and then restore this at a later date. |

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| Requirement | Justification |
| Sliding scale for adjusting the speed of the simulation. | A sliding scale is easy for a user to adjust, and precise values are not required. It is intuitive and simple to understand, rather than requiring the user to enter a specific clock speed to use. |
| Visualization of the register contents of the PC, MAR, CIR, MDR, ACC | These registers are an important part of the specification and understanding of how a processor works, therefore they should be visually distinct from the general-purpose registers. This makes the interface easy to understand. |
| Example Bubble Sort and Binary Search | Bubble sort and Binary Search are of significant complexity to aptly demonstrate the abilities of the processor and instruction set. They are also key algorithms included in the Computer Science course, so users may already be familiar with them. |
| The editor must highlight unknown mnemonic, as well as cases where the mnemonic is not followed by the correct amount of parameters. | This simple analysis of the code written by the user will sufficiently catch a majority of mistakes made and assist them in writing correct assembly first time. It will not be too difficult to implement. |
| TO BE EXPANDED |  |

### Requirements

### Success Criteria

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| Success Criteria | Justification |
| Sliding scale should correctly adjust the speed of the simulation from 1Hz to at least 100Hz | 1 Hz to 100 Hz provides an adequate range of test values to ensure that the simulation correctly scales to the different speeds. There shouldn’t be much need from users to run it faster. |
| The contents of the PC, MAR, CIR, MDR, ACC should be displayed accurately and real-time, ensuring the view and model in sync. | It is important that elements of the interface accurately represent the state of the model being simulated in the back-end. |
| The contents of the PC, MAR, CIR, MDR, ACC should be adjustable via the interface and this adjustment should have the correct effect on the simulation. | Bubble sort and Binary Search are of significant complexity to aptly demonstrate the abilities of the processor and instruction set. They are also key algorithms included in the Computer Science course, so users may already be familiar with them. |
| TO BE EXPANDED |  |

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# Section 3: Development

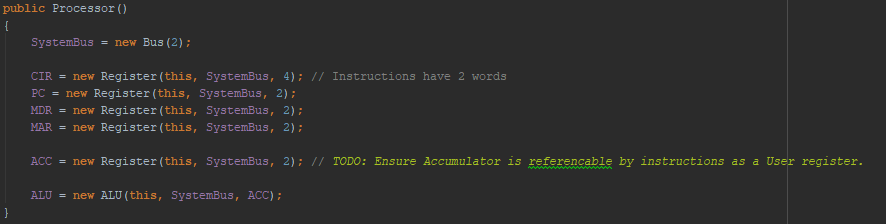
## I decided to break my development down into several individually testable stages. At each point I would be able to review the functionality of the code I had just written, as well as retesting code that this code relied on to prevent regression.

At the end of each stage of development, following a brief description of the functionality of the code written, I will include the test tables detailing the test, expected result and actual result as well as any debugging and bug-fixing that occurred as a result of the testing.

## Wire Framing the Classes

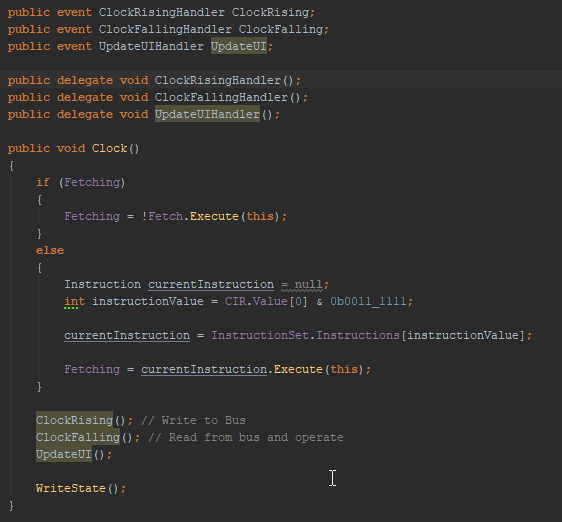
I started off development by creating a handful of classes and wire-framing their properties and methods. Whilst the code written would not reflect the final implementation of the classes, it would be enough to see how it would fit together and evaluate how effective the structure would be.

The first class I created was the processor class. This class would consist of other components and tie them together in a hierarchal structure. The processor class would act as the model that would eventually be interacted with and displayed through the view layer. By passing the processor to the sub-components, they would be able to easily access other components. This technique is clear within the constructor of the processor class:



Here you can see the instantiation of a variety of registers, linking them to the processor, system bus and specifying their width in bytes.

The processor works on an event-driven model, with each Clock tick triggering three events ClockRising, ClockFalling and UpdateUI. These events are listened to by the individual components which then act accordingly. I decided to use events as they provide a flexible way of triggering methods across a range of dissimilar objects.



Here the three events and their corresponding delegates can be seen. These are scoped as public because the other classes (the view and the components) also need to be able to hook onto these events.

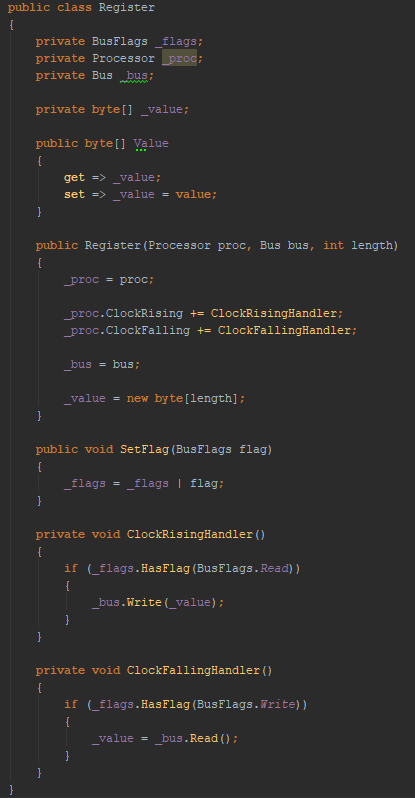
A rough implementation of the Clock method can also be seen. The Fetching flag simply refers to if the application is in the Fetching or Executing part of the cycle. The instruction class provides a simple Execute method which returns True or False whether or not the instruction has completed each of its micro-code steps, this will become clearer later in this section when the Instruction class is shown. Also notable is the inclusion of binary masking using the AND operator to select the operation code part of the instruction.

The final part of the processor class is the hard-encoded Fetch instruction. Whilst the instruction set will be inter-exchangeable, the Fetch instruction is not available to the user and instead used only internally by the processor. I drafted the fetch instruction based on the specification I processed for the EDP.



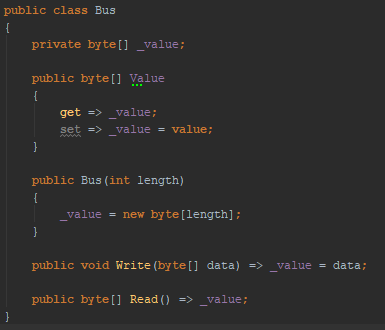
Each stage in the array represents a microcode instruction that sets the flags on each of the registers and components. The Fetch instruction is interesting because it has to retrieve two words from the memory. This means two memory operations are completed, one for the first word and one for the second. A rough comment is included for each step that shows the transfer of data between registers.

I then had to write the basic implementation for the registers. Like all other bus components they would be designed to write to the bus on the rising edge and read from the bus on the falling edge. This emulates an actual system where it takes time for the signal to physical propagate across the bus.



The class is relatively simple. During construction it hooks onto the rising and falling events and initializes the internal array. I decided that byte arrays would adequately fulfil the needs of the application as they can be indexed at each byte, just how actual memory would work. A flag enum is used for controlling the state that mimics the behavior of control lines in the actual processor.

The bus component is even simpler with the registers simply directly writing to it on the clocks rising edge. If more than a single register writes to it, then it will be overwritten and not merged as we might expect to see on actual physical hardware, although this is an edge-case as two registers should not simultaneously write to a bus.



As part of allowing further extensibility, there are two ways of writing or reading to the bus. The value can either be directly interacted with via a property or via two functions. The Write and Read functions may eventually provide more complicated logic for correctly handling a register with a shorter width writing to the bus.

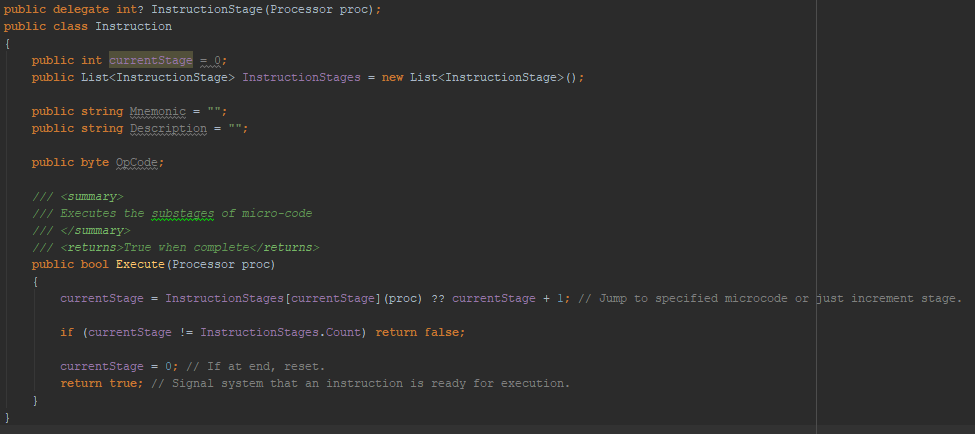
The final class needed as part of the processor components was going to be the ALU. This would need to interact with the bus as well as directly accessing the ACC. I decided to implement a basic add function, as well as two specialized ones that increment in word lengths. Similar specialist hard-coded functions can be found in modern processors, allowing the fetch-decode part of the cycle to take up less of the overall processor time.



The ALU acts similarly to the rest of the bus components, being driven by the two clock edges as well as being primarily configured via a set of flags. One primary difference is that it has a direct interaction with the accumulator without having to cross any busses. This is convenient and allows the processor to complete basic arithmetic in less cycles.

For ease of development, I decided to cast the byte-arrays to Int16s for the purposes of arithmetic. This meant I did not need to write the underlying logic of the ALU, as this would have been time consuming for little additional benefit.

The final classes I wire-framed were the abstractions for the Instruction and Instruction Set.

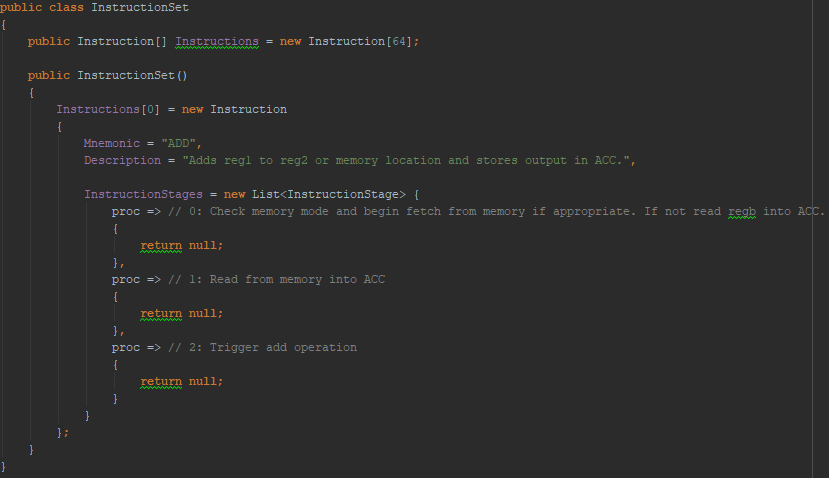


The instruction class represents a single assembly instruction. It is used both by the processor for processing the instruction via the microcode steps provided in InstructionStages and will also later be used by the assembler when converting from mnemonics to bytecode.

The execute function simply steps over each of the microcode steps and returns a true signal to show that the entirety of the microcode for that function has been completed. If it returns false, the processor should continue to execute that instruction until all of the microcode has been executed. Returning true will usually force the processor to return back to the fetching state.

The instruction set class acts as a wrapper around an array. It contains each of the possible instructions. The advantage of making this a class is that we are able to offer multiple instruction sets in the future that can easily be swapped out in both the assembler and the processor. This may allow an instruction set that mimics RISC like behavior and an instruction set that mimics more CISC like behavior with more comprehensive instructions.

Alternatively this could have been implemented with a static class, but this would not have offered the ability to change out the instruction sets so easily. I chose an array as the datatype as the instruction set will not grow in size during execution and the array type allows single operation reads to any element of the array.



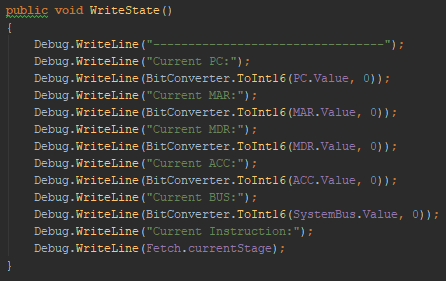
### Testing

The scope of the testing as this stage is limited as the application is very simple, but it is useful to test the initial stages to ensure they are correctly implemented before building upon them.

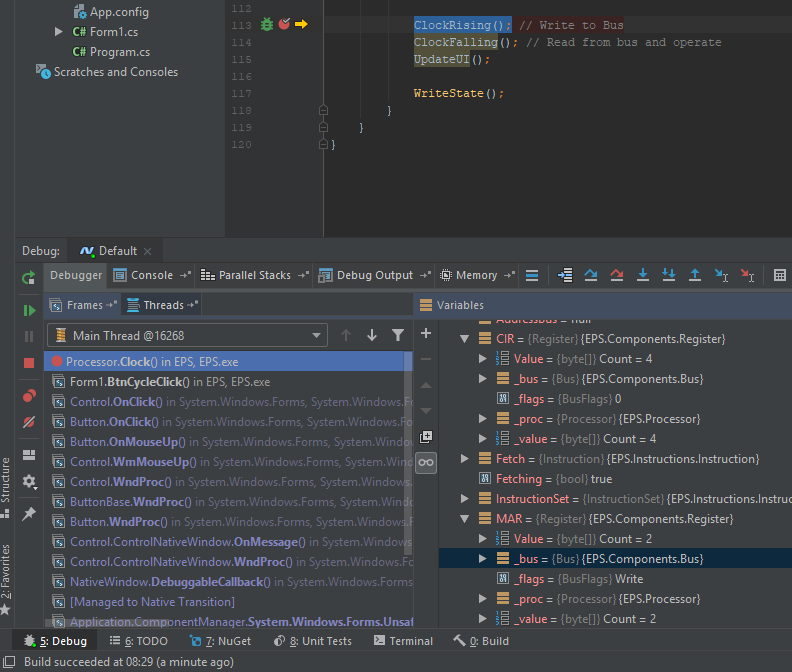
|  |  |
| --- | --- |
| Test | Expected Result |
| Allow the application to tick through the fetch cycle repeatedly | We expect to see the 5 distinct stages of the fetch cycle being correctly executed. This can be seen with the contents of the registers. For example, we expect at the end of each cycle for the Program Counter to have incremented by 4. |

### Bug Fixes

During testing I noticed some unexpected behavior. The Program Counter was setting itself within the cycle to various numbers and seemed to be stuck at a certain point. It looked as if the central control of the processor was entirely flawed, as several of the registers seemed to be doing their own thing, not heeding the flags being sent out by each stage of the processor. I decided to implement a basic debug routine to help show me what was happening in each of the registers to work out why it was not working.



Having implemented this I realized that the registers were successfully completing the first few iterations before being caught in some weird loop of simply repeating the same action. I realized that in order to debug this further I would need to make use of the built in runtime debugger within Rider, my preferred .net IDE. Runtime Debugging is very effective compared to simply printing values as you can more carefully step through and view all of the values within the scope, in some systems you may even modify the value of the variables. I placed a breakpoint inside of the main loop between the clocks so it would be possible to see the flags of each of the registers at the end of each application of the instruction.



It quickly became apparent using the runtime debugger that the register flags were not being reset and were instead accumulating. This meant that the first few iterations of the system would behave as expected before it would begin to diverge from the expected values. This prompted me to check if I had implemented a reset mechanism for the flags, and I realized that I had not. The problem was shortly resolved by setting the flags on all of the components of the processor to 0 at the end of each cycle.

I then decided to redo my tests, this time focusing on the expected changes in the registers. I calculated the expected value of each register based on the operations that should occur in that phase of the cycle, and compared this to the actual running application to verify that the entirety of the processor was working correctly.

|  |  |  |  |
| --- | --- | --- | --- |
| Step | Register Operation | Expected Value | Actual Value |
| 0 | PC + 2-> ACC PC -> MAR | 2  0 | 2  0 |
| 1 | MDR -> CIR | 0 | 0 |
| 2 | ACC -> MAR  ACC + 2 -> ACC | 2  4 | 2  4 |
| 3 | MDR -> CIR[1] | 0 | 0 |
| 4 | ACC -> PC | 4 | 4 |

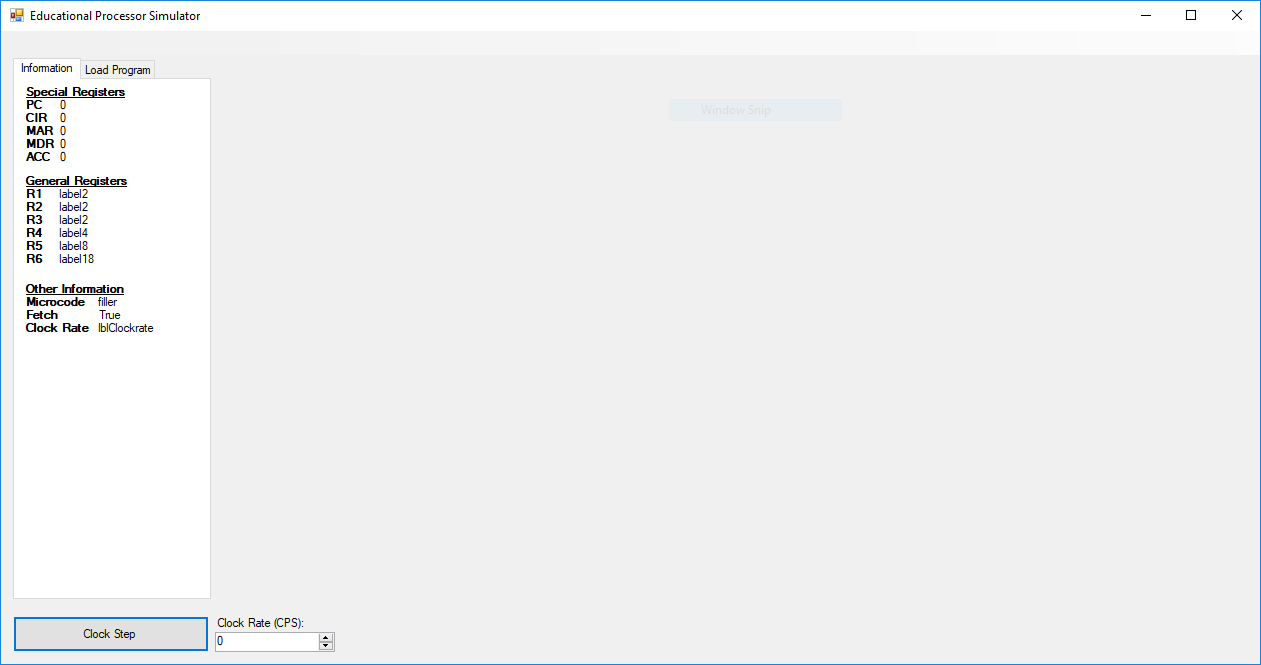
The tests seemed to indicate that the processor was now correctly orchestrating the registers for the purposes of loading a new instruction to execute. This meant I would then be able to move onto producing a rough UI that would show the state of the processor.

## Producing the rough UI

By the end of this task there should be a rough UI that will be able to control the processor and display the memory. Also as part of this part of the development, I will work on the memory and interfacing that to the MAR and MDR.

Whilst I primarily write code in Jetbrains Rider, for this task I switched to Visual Studio as this provides a helpful WYSIWYG editor that allows much more rapid development and prototyping for UI.

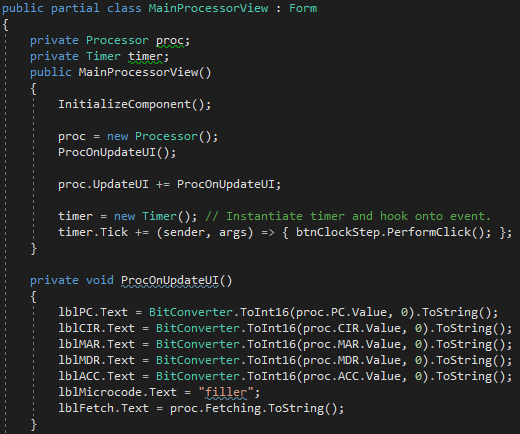
I first drew up a version that was purely UI and was not bound to any data. I could present this to the potential user base to see what they thought of it. My first prototype did not include the memory display as I will still thinking of several different ways of implementing this. It needed to be flexible and concise as it would have to show or be capable of showing what is quite a large data set. So, I left a blank area that would eventually be filled with my prototype for showing the memory.



It follows the general convention of application layouts with a space left for a toolbar at the top and a tabbed display on the left hand side. This allows more information to be included in a view without cluttering it, as you only show information relevant to the user’s experience at that time. I started off with two tabs, one for displaying information about the processors current state and another that will eventually hold the controls for loading a program and data into the memory.

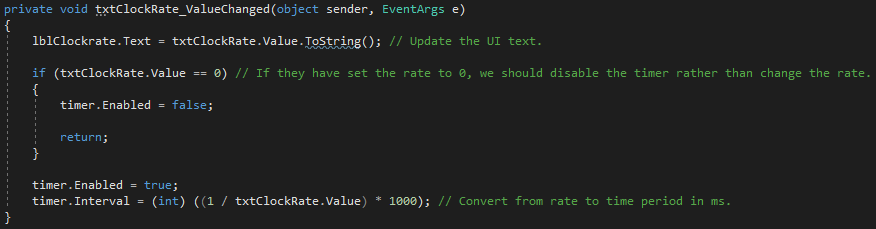
Controls such as the speed and manually cycling the clock are displayed in a space at the bottom. This is because I expect the user to want to always be able to easily access these and placing them within a menu structure would overcomplicate the experiences and slow down the user when they are trying to complete a task.

Hooking these into the actual data model was quite easy due to the modular design. I was able to extend the clock system to include a third and final stage “UpdateUI” which triggers the application to update the view to show the now changed data of the model after the rise and fall of the processor. I may want to change this behavior eventually so that it shows the Rise and the Fall separately to clearly demonstrate to an end-user how this specific functionality of the processor works.



Here we see that the Form instantiates a new processor object and then hooks into the UpdateUI event to trigger the ProcOnUpdateUI method. This goes through each of the UI elements and sets them to the value from the processor. As this function continues to grow, it may make sense to investigate only updating specific parts of the UI, or rate-limiting the updates. If the processor is running at 100hz, it may make more sense to only update the UI every 10 frames otherwise it will put a strain on the host machine which may become slow and unresponsive.

The Form also drives the processor using the built-in .net Windows Form Timer. I decided to use their implementation of the Timer as I doubted that I would require anything unusual or specific that would warrant writing my own Timer system. The Slider on the UI then hooks into this to change the interval of the Timer.



The logic also includes a simple test to make sure we disable the Timer when they have selected 0 Hz and then return out of the method. If we didn’t then a DivideByZeroException would be thrown when we try to complete the math on the last line.

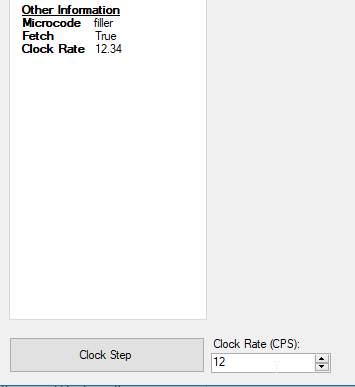
### Testing

With the core functionality of the model already tested, we now need to make sure that the same values are reflected within the UI. There are also a few more elements to be tested including the clock step button, and the clock rate entry.

|  |  |  |
| --- | --- | --- |
| Test | Expected Result | Actual Result |
| Pressing “Clock Step” and checking results via debug | This should cause the application to iterate through one clock cycle. In this case we should see the various registers behaving as they did in “Wire Framing the Classes” testing. This means when the fetch instruction completes (5 clock cycles), we should see the PC displaying 4. | When clicked 5 times (the length of the fetch instruction) we see the PC increment a full 2 words to display 4. |
|  |  |  |
| Pressing “Clock Step” and checking the results via the UI | The UI should match the data that is shown within the debug tool as tested above. | The view correctly matches the data within the model and shows 4 as the value for Program Counter. |
| Setting the Clock Rate to 0 | The Clock Rate displayed on the UI should be 0, and it should not clock the processor. | The processor does nothing as expected. |
| Setting the Clock Rate to 1 | The processor should slowly (1 per second) clock itself and this should be visible by the changing values. | The values change as expected, without direct interaction from the user. |
| Setting the Clock Rate to 100 | The processor should increment the registers as expected and remain responsive. | The processor increments as expected without interaction from the user and host machine CPU usage increase minorly but the application remains responsive. |
| Setting the Clock Rate to 666 | The field should, as configured, cap itself to a maximum value of 100 and reset to 100 after any unacceptable values. | The field immediately changes back to 100 after being set above this limit. |
| Setting the Clock Rate to 12.34 | The Clock Rate should round down to 12 and the UI should show this. | **The Clock Rate sets itself to 12.34 but the Clock Rate entry box rounds down to show 12. This means the UI is inconsistent in handling Decimal Places!** |

### Bug Fixes

Whilst most of the testing was successful, it did discover a inconsistency in the way the UI displays information. The selection box for the Clock Rate allows a user to enter a decimal value, and holds this value but by default only displays it as an integer. This means that whilst the value was actually 12.34, the user thought it had been rounded down to 12.



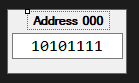
Resolving this was as simple as changing the ValueChanged method to begin by using Math.Round to set the value. This meant it was not only rounded in the data, but also correctly rounded in both the sections on the UI where it is shown

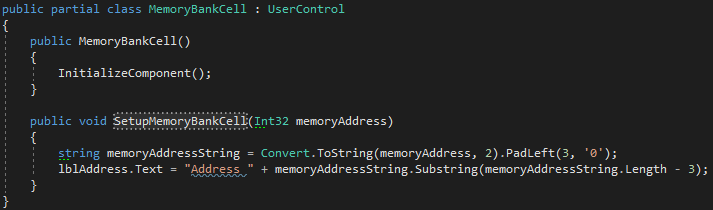
## Producing the Memory Bank UI

I felt that I would need to create the memory UI separately from the rest of the UI components because it had sufficient complexity and design requirements that it would need separate, specific and detailed testing.

I knew that this part of the UI would require lots of repeating elements and hence in the spirit of DRY (Don’t Repeat Yourself) I decided to break it down into three elements, so that code could be reused effectively. First, I would develop the individual cells that will display a byte or single address of memory, then the row that will contain those and finally the overall MemoryBank container that will set up the rows and organize their layout.

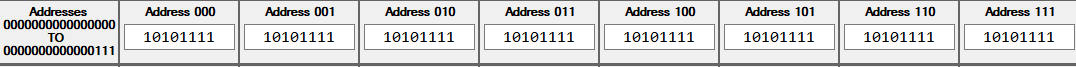
The MemoryBankCell is a relatively simple unit that contains a text box, for now filled with dummy data to show what it could look like, as well as a label that indicates the address of that byte.



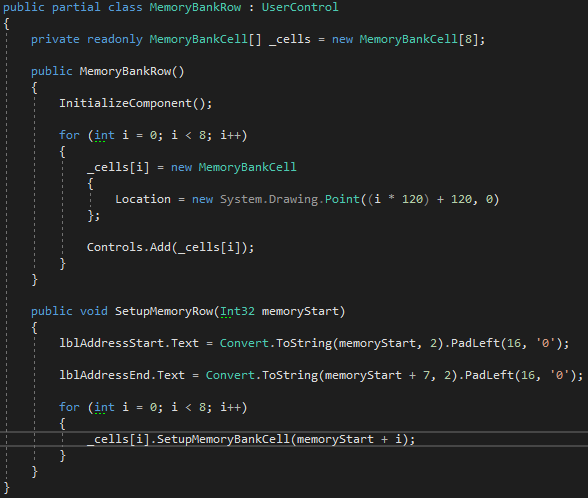


The code for this element is relatively simple however there is one interesting point. I was presented with two possible options: setting up the memory cell within the constructor, or providing this as a separate function to the constructor. The advantage of placing the setup in another function is that it is then possible to change the memory address represented by the cell on the fly, if it had remained in the constructor then our application would have to tear down the object before creating and rendering the new one.

Next I built the MemoryBankRow. This would wrap the cells in a row and provide to them their individual memory addresses. Eventually the main wrapper will pass the start address to each row. This tree of dependency means that it is incredibly easy to change the section of memory being displayed on the screen, as a change can propagate from the wrapper, to the row, to the child cells simply by invoking a single function on the wrapper.

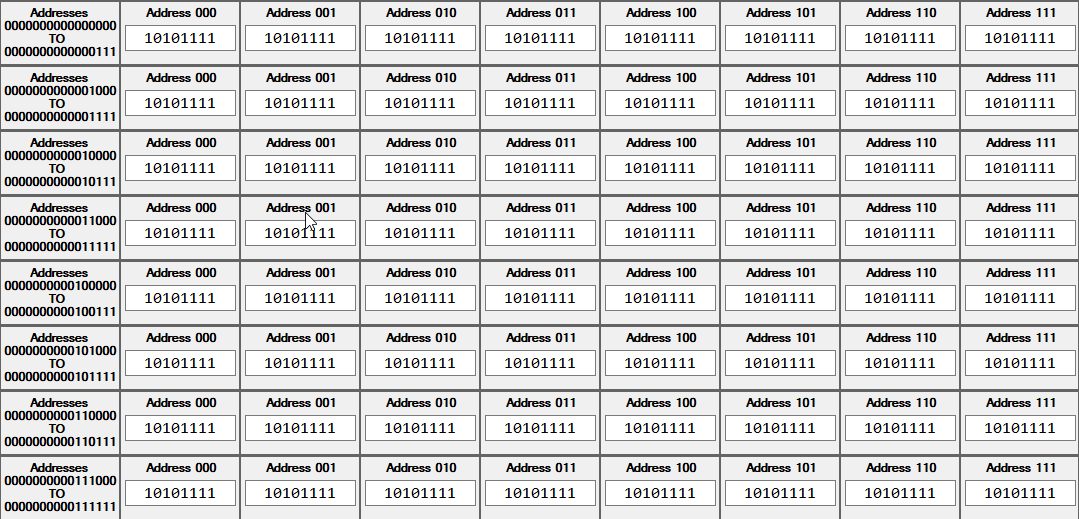


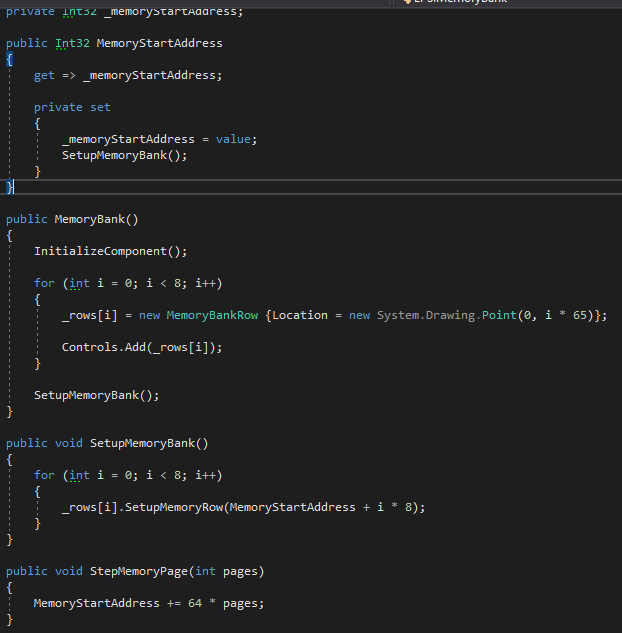
For this early prototype, I decided to use binary addresses and at a later date add in support for switching to a hexadecimal display. Hexadecimal would make it possible to display the entire address (16 bits) instead of just displaying the last three bits in the context of the row. This is because a single hexadecimal digit can be used to represent four bits, meaning only four digits could be used to represent the entire sixteen bits.



Again we see a relatively simple structure behind the component, as it only has to instantiate the eight cells and be able to pass information down to them as well as formatting the address range it represents to show as 16 bits. I use fixed length arrays to hold the MemoryBankCells as I can be sure that there will always be 8 cells and by using arrays access to data is faster and the data itself takes up less space than other data structures such as Linked Lists.

Finally we have the container that will hold the rows. It will also control the pagination of the memory bank so the user can switch through each page of 8 rows of 8 cells (64 memory addresses). Whilst the buttons for this interaction will be outside of the class, they will be able to interact with it through public methods. This is an example of encapsulation as objects outside of the MemoryBank will not be able to directly access the private properties such as the memory address being targeted, instead these private properties will be manipulated through public methods such as nextMemoryPage() which can have additional logic to ensure that only valid data is selected, for example, ensuring it is not possible to go past the end of the possible memory address range.

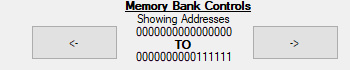




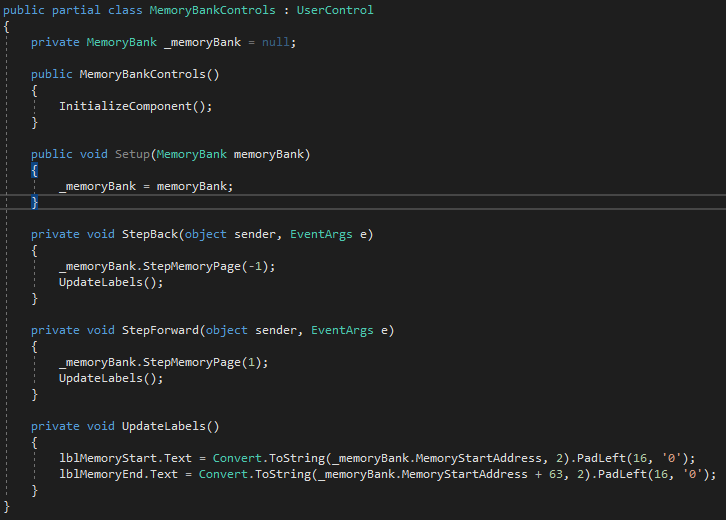
Again, we can see this this component simply builds upon the previous components and hence maintaining its simplicity. The code demonstrates the use of a getter/setter in order to maintain encapsulation as well as to trigger another function when data does change. The function is this example will propagate the change down to the rows, which will propagate it down to the cells.

The StepMemoryPage public method will be used by controls outside of the memory display to interact with it.

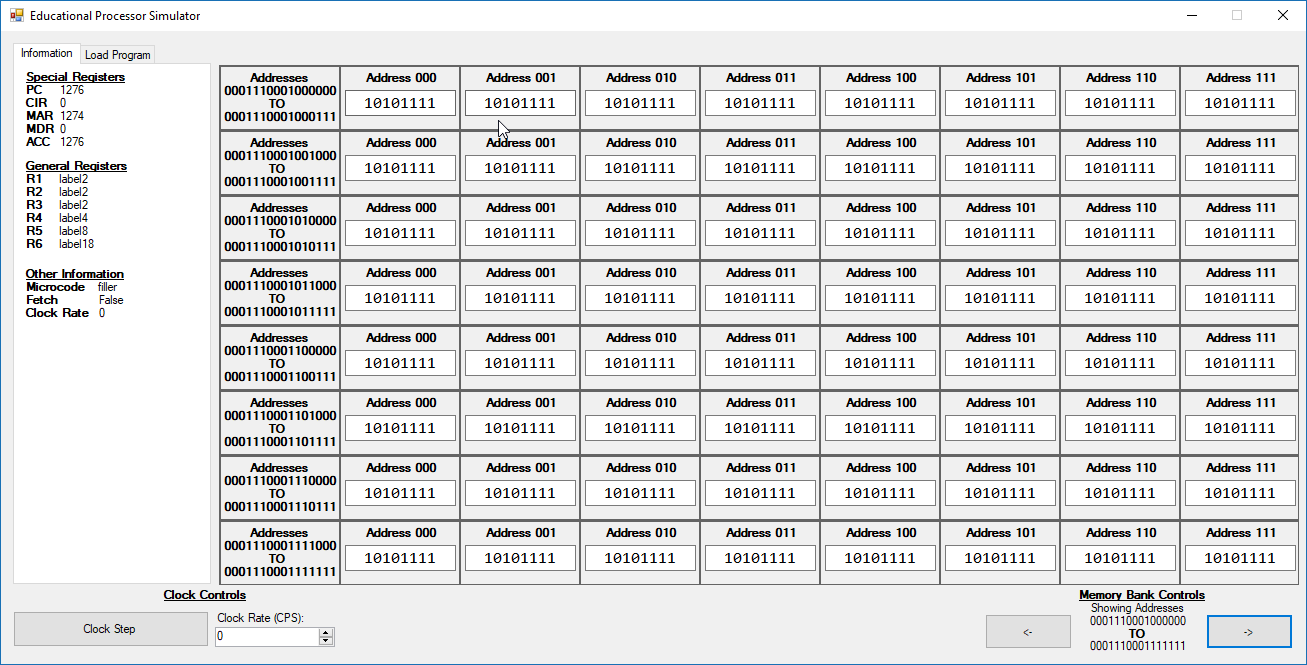
The final step before I could complete more testing was to link up some controls within the interface.



I created this unit as part of its own control because this would keep the code separate making it cleaner and more maintainable, this also meant that it would not have special or particular access to the MemoryBank, instead only interacting only through the public methods available.



With all of the components complete, the UI for the main window now looks as follows:

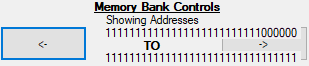


### Testing

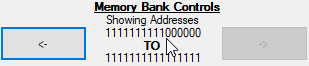
Whilst the Memory Bank UI has not yet been tied up to the data model, it is still possible to check that the address labels and interaction buttons work as expected.

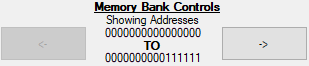
|  |  |  |
| --- | --- | --- |
| **Test** | **Expected Result** | **Actual Result** |
| The original state of the UI is correct before any user interaction. | At start, the memory bank should show addresses 0000\_0000\_0000\_0000 to 0000\_0000\_0011\_1111 with 8 unique addresses presented on each row. | The address ranges of the entire memory bank as well as the individual rows match what is expected. |
| Clicking the next page button from the original state. | The range of the memory bank should change to 0000\_0000\_0100\_0000 to 0000\_0000\_0111\_1111 and the address range of each row should fall within this. | The memory bank correctly shifts to the next page of 64 addresses. |
| Clicking the next page button again. | The range of the memory bank should change to 0000\_0000\_1000\_0000 to 0000\_0000\_1011\_1111 and the address range of each row should fall within this. | The memory bank correctly shifts to the next page of 64 addresses. |
| Clicking the previous page button. | The range of the memory bank should change to 0000\_0000\_0100\_0000 to 0000\_0000\_0111\_1111 and the address range of each row should fall within this. | The memory bank correctly shifts to the previous page of 64 memory addresses. |
| Clicking the previous page button from the original state | The user is not able to move the memory bank back another page. | **The memory address goes into a negative value.** |

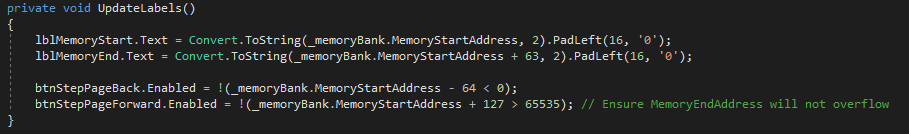
### Bug Fixes



As seen in the screenshot here, we have failed the test suite. This is definitely not a good user experience and some data validation needs to be implemented to ensure it is not possible for a user to scroll back before the acceptable range of memory addresses. To resolve this some basic data validation needed to be added. In my case it meant disabling the button to make it clear to the user that interacting with it would not produce any results. This is preferable to simply having the button do nothing as this might be confusing to a potential user.







Demonstrated is the MemoryBankControls at either end of the two extremes, where it would be able to cause it to go into the negative, or cause the memory address to overflow. We can now see that a visual indicator (the greying out of the control) clearly shows the user that the control cannot be interacted with. This was implemented simply by considering the memory address each time it has been incremented and whether or not it would go into the negative if the page was moved back and forth. Now that this has been completed, the test suite now passes and I can move onto producing the memory bank model.

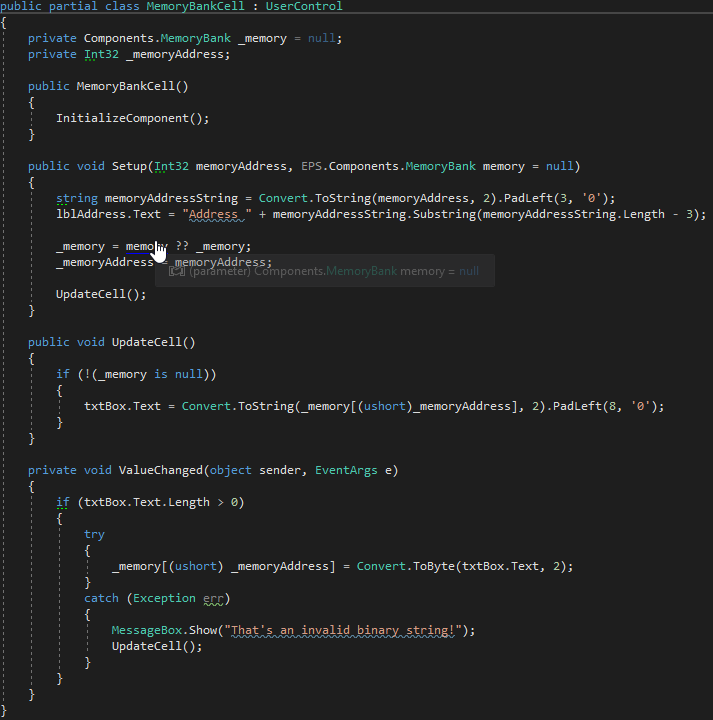
## Producing the Memory Bank Model

As previously explained, I decided to break this stage separately from producing the UI as both are independently testable.

The Memory Bank will emulate the behavior of RAM, reading the address supplied by the MAR and placing this data inside of the MDR. I have decided for the purposes of this processor for the latency of memory read and writes to be instant and occur within a single clock edge in the same way that the registers behave. This abstracts away some of the complexity typically involved with reading and writing from memory that exists outside of the processor itself.



Similar to the Registers, we see the component acts mainly on the falling clock signal and uses a set of flags to control its operation. One interesting thing to note is the inclusion of an ‘indexer’. An indexer is a feature of the C# language that allows the developer to specify getters and setters for when the Object based on a class is indexed. This allows the developer to create custom data types similar to arrays or dictionaries, and in this case other components will be able to access the memory via MemoryBank[address] as will be demonstrated later. This further shows the flexibility and power of OOP.



Here we see the binding of the individual MemoryBankCell to the MemoryBank model. We can see that a try catch is used as the default behavior of the Convert.ToByte is to throw an exception if the string entered is either too long to fit into that height or will not convert to a byte cleanly. If the user does enter an invalid string, we show a message to let them know and then reset it to the value of the cell from before they attempted to change it.

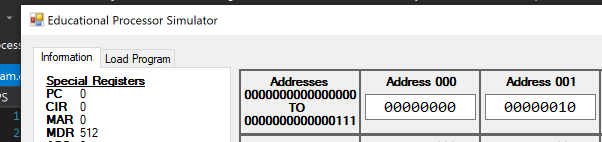
### Testing

|  |  |  |
| --- | --- | --- |
| **Test** | **Expected Result** | **Actual Result** |
| Cells should display correct initial value. | Cells should display 00000000 on initial load. | https://ss.noahstride.co.uk/screens/2019/01/EPS_2019-01-07_21-50-18.png  **Correct Result** |
|  |  |  |
| Entering a valid binary byte into a cell. | The user should be able to enter a valid binary byte and this value should persist when the user clicks out of the cell. | https://ss.noahstride.co.uk/screens/2019/01/EPS_2019-01-07_22-00-27.png  **Correct Result** |
| Entering an invalid binary byte into a cell | Upon entering a character that will not convert properly to a binary byte, the application should display a warning message to the user, and reset the cell when closed. | https://ss.noahstride.co.uk/screens/2019/01/EPS_2019-01-27_13-50-56.png  **Correct Result** |

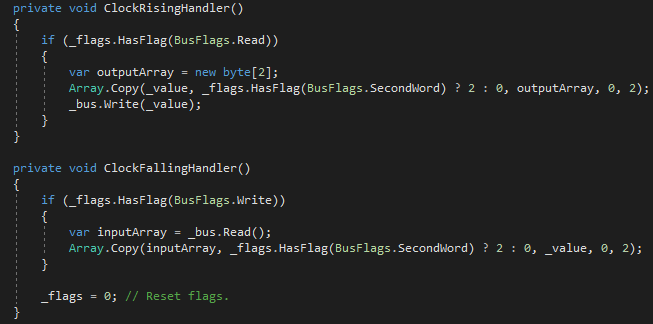
Because of the modular design, it is now possible to test the interaction between the memory bank module and the rest of the processor and to ensure that everything works together correctly.

|  |  |  |
| --- | --- | --- |
| **Test** | **Expected Result** | **Actual Result** |
| Entering a value into a cell, and allowing the MAR to select this address | The MDR should show the value of the cell as 2. | A value of 512 is shown.  **FAIL** |
|  |  |  |

### Bug Fixes



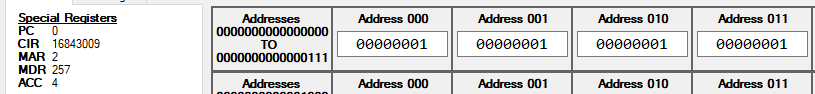
This result was rather un-expected, however, it quickly began to make sense why it was behaving this way. As part of the load cycle we expect the processor to load in 32 bits of memory (2 full words) into the CIR, here we instead see two things going wrong. I used my IDEs run-time debugger to step through the cycle to confirm my suspicions and upon inspecting my source I realized that the second word loading/writing of the CIR was not fully implemented and this meant we were only pulling in 16 bits of the expected 32 bits. This was quickly rectified within the ClockRising and ClockFalling handlers:



I made use of the ternary expression (?) here to ensure that the code remained short and concise and to enable maximum effective re-use of code.

The second issue I noticed as a result of this test was a mismatch in the byte orders. I was expecting the processor to operate in Big-Endian order and this means that the largest byte in a value comes first, this is common in older processors, but has been phased out in preference of Little-Endian order. The built-in C# converter assumes that byte arrays will be in Big-Endian order. This means that the values of the numbers are scrambled compared to what a user might be expecting, I decided to leave this for now as it made more sense to leave it displaying this way, if that is how the processor is actually handling the value.

With these resolved, the CIR now shows the correct value.

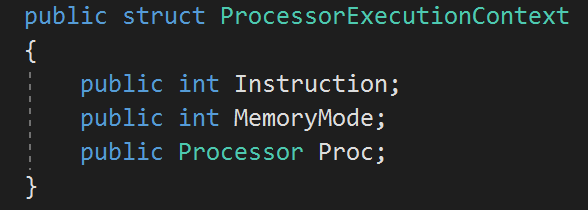


## Adding Instructions

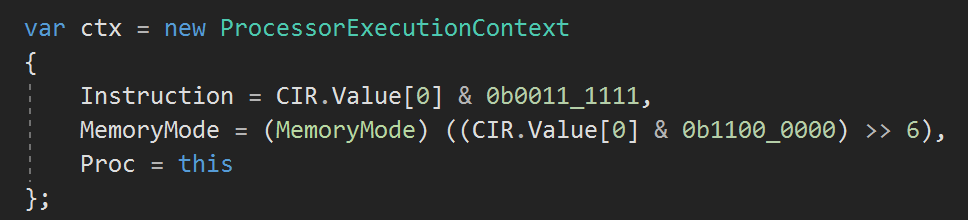
With the basis of the processor complete, it was now possible to implement several instructions for the user to use.

I decided that for the processor to be able to display basic functionality I would need to implement at least ADD, LDA, JMP and BRA, BRZ and BRP.

To begin, I needed to introduce a context struct that would describe the state of the processor so that each stage of the execution of an instruction has access to the information it needs to complete. Whilst a simple structure, it allows a much cleaner approach to providing general information to the steps of execution without polluting an existing namespace.

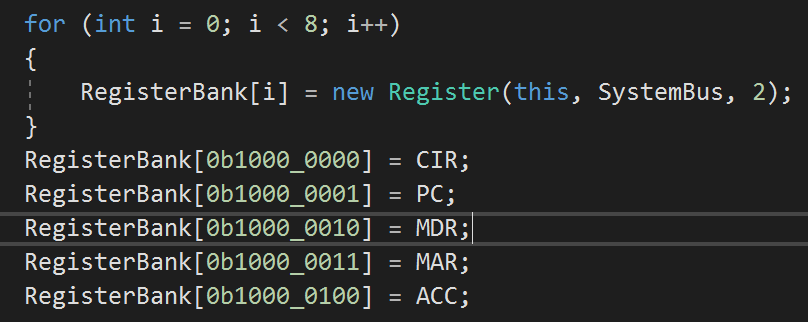


These values are then filled within the execution cycle before being passed to each step of execution. Also demonstrated here is a binary bitwise AND followed by right shift in order to convert the full instruction to just the memory mode. This is cast to the appropriate enum to keep the code clean.



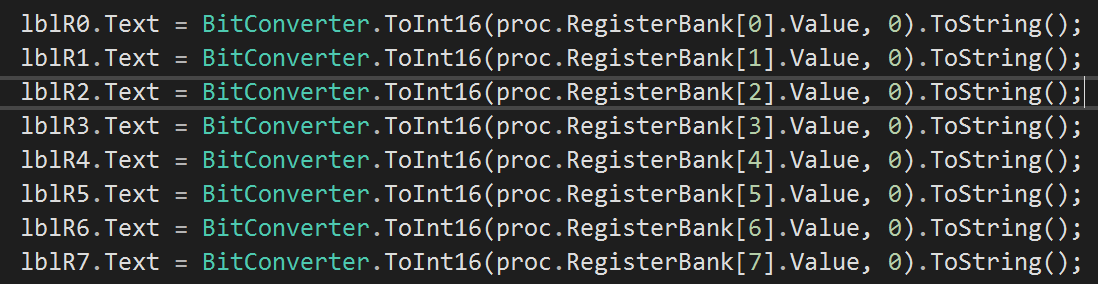
As well as producing the struct, I then needed to add the context where appropriate to replace direct calls to proc.

I also needed to implement the general registers, as well as a way of appropriately accessing them. I decided that a small 8-bit address space would allow the general registers as well as the special registers to be accessed by users’ applications programmatically.

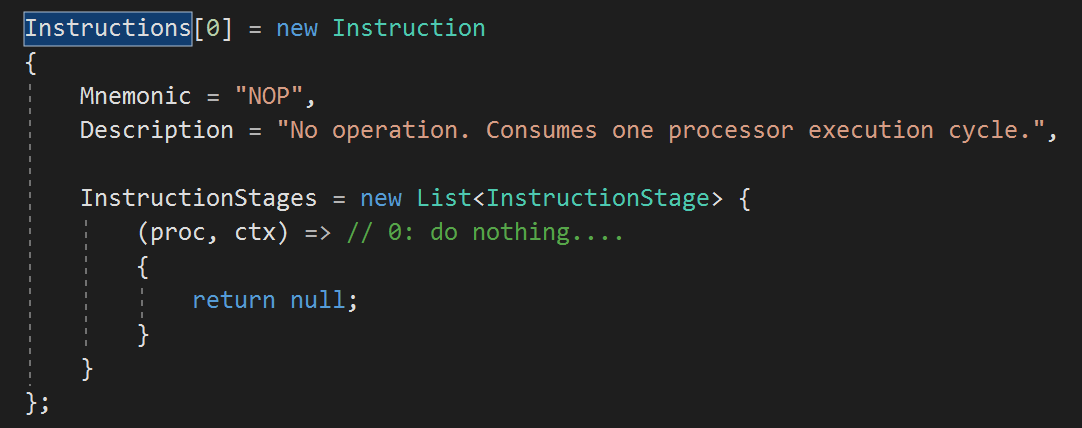


By adding these registers to a bank (in this case represented by an array) the user would be able to specify any of these registers (the general and special) when writing their machine code. I felt an array was a suitable data-type to choose since it would always have a fixed length. As I knew it was a fixed length I was then able to use the first bit to represent whether or not the program wanted to access a special or general register.

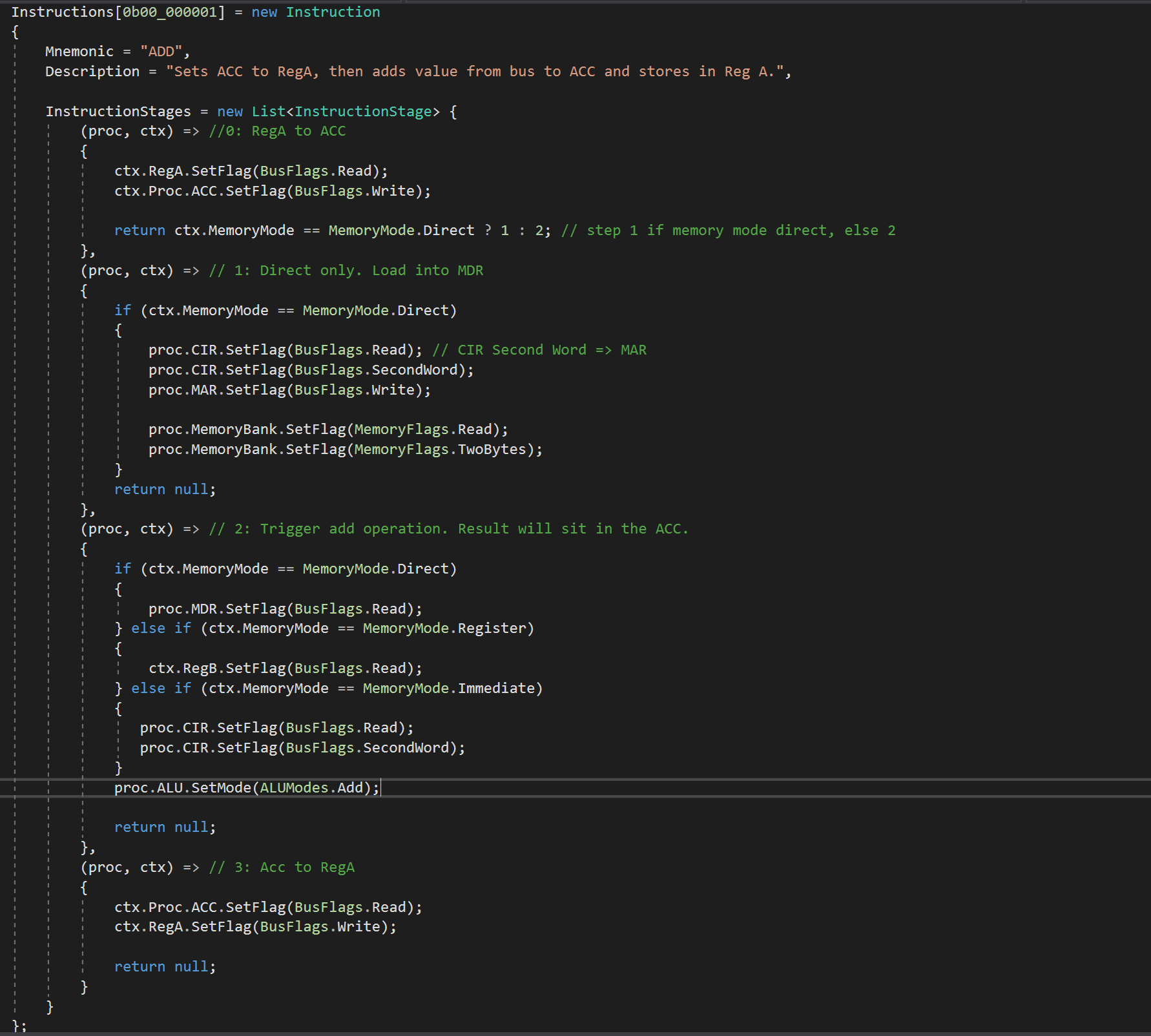
In addition to adding the data side, I also needed to add these registers to the view presented to the user. This was relatively simplistic due to the existing framework for mapping values I had created.



The first instruction I wrote was NOP (No Operation) as this was the simplest. Despite being simple, it is still an incredibly useful instruction in certain circumstances such as where it may be preferable for the processor to wait several cycles before completing an action.



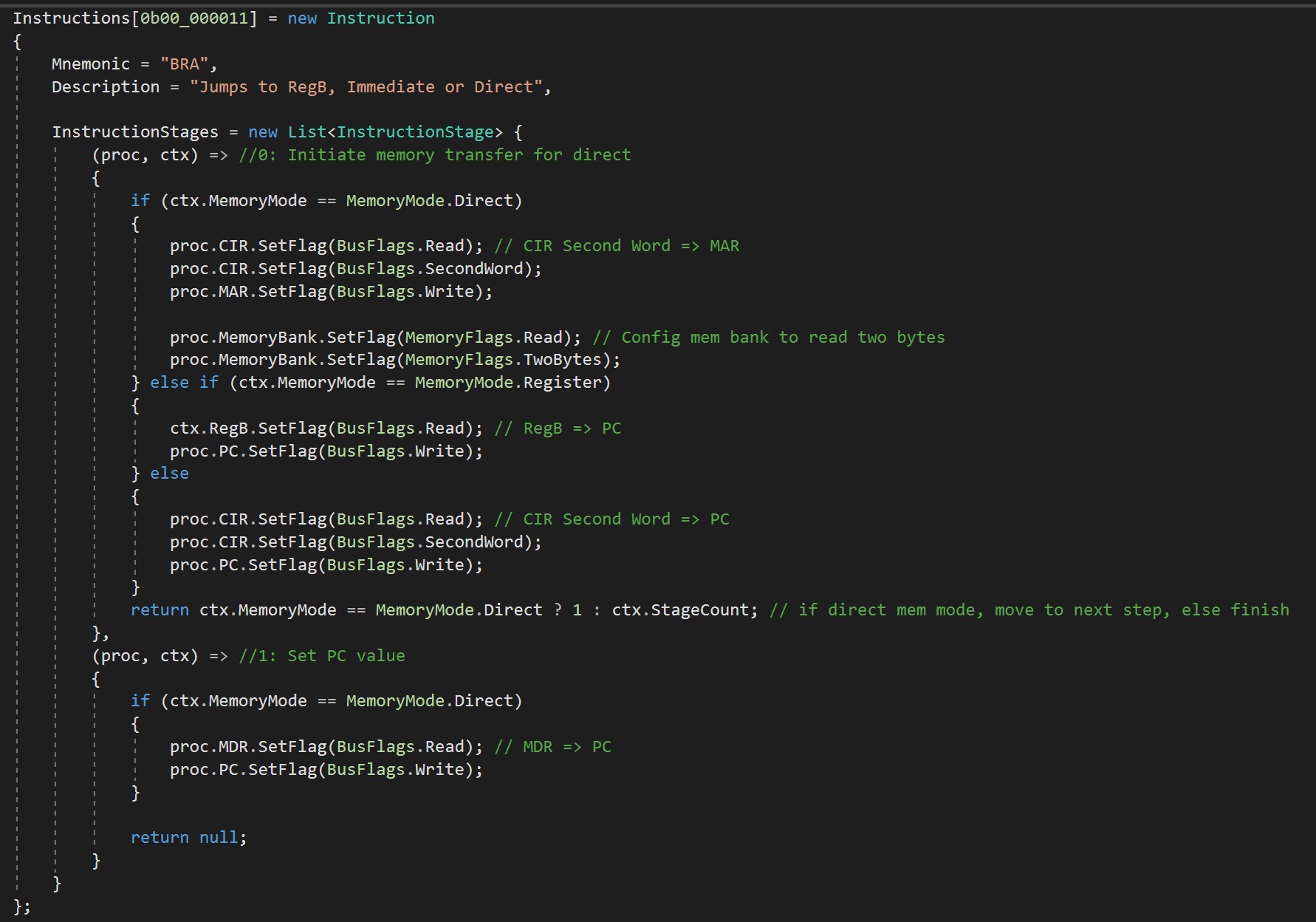
The next instruction I needed to implement was the Add instruction. It would need to be able to handle three distinct scenarios: direct, indirect and register read.



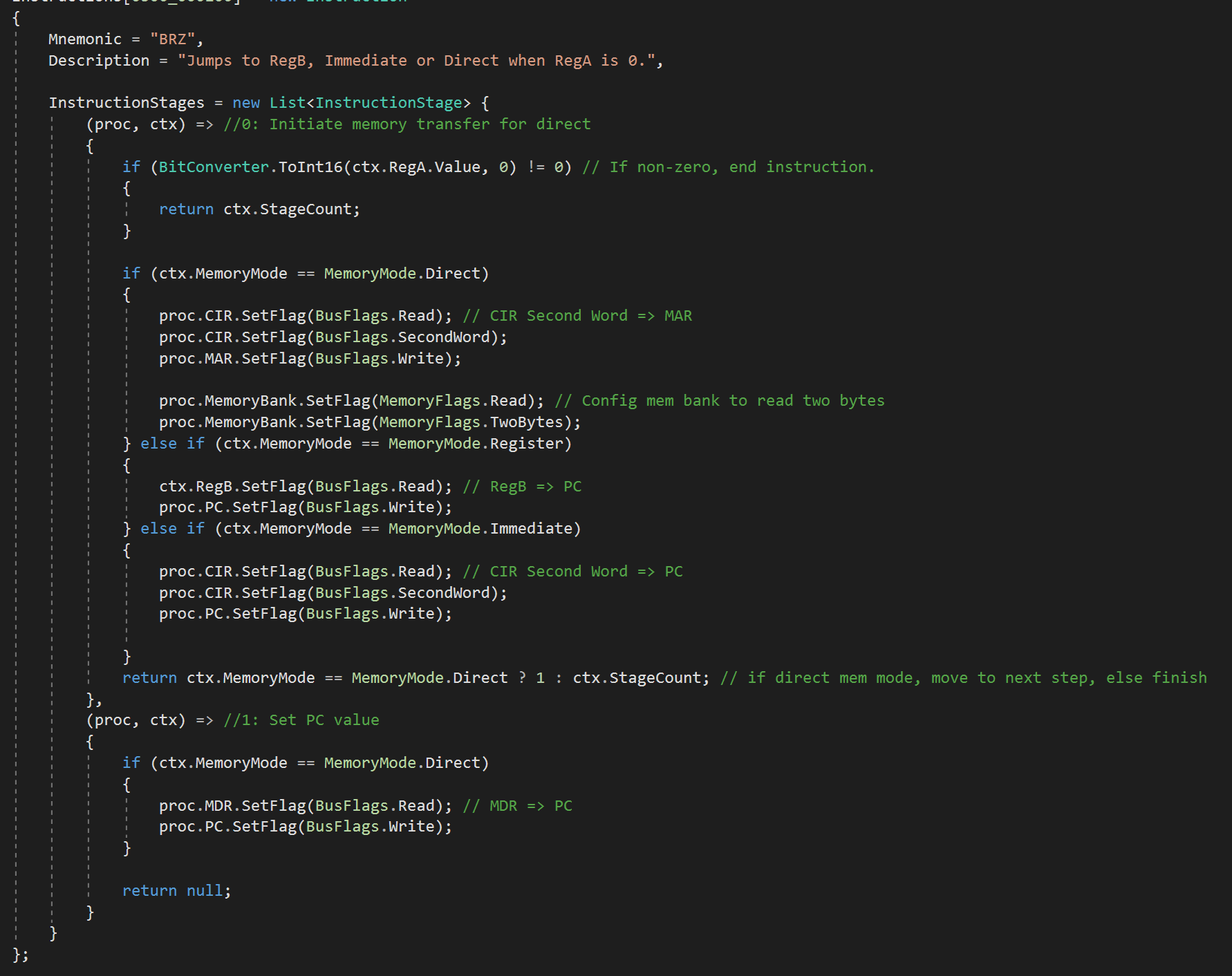
The add instruction completes within 4 cycles and has a relatively simplistic design making use of the micro-code framework I had previously developed. I also commented each stage of the instruction to make clear to myself and other developers the purpose of that step, since it is not always immediately clear what it intends to do. Even with the handling of the three memory modes, the code remains relatively concise due to the structure provided by the framework.

The next instruction I developed was the SUB instruction as this was just a small modification required to the ALU class itself as well as the just copying and making a small change to the addition instruction.

Then the next instruction to develop was BRA. BRA allows the user to tell the processor to jump to a specific memory location by setting the PC to that location. Theoretically this could have been completed with just a MOV instruction, but it makes more semantic sense to the user for it to be a separate command, and it will also be a foundation for BRZ and BRP. We can see that once again, the micro-code for each instruction becomes quite lengthy when we consider all three of the possible memory modes.



With BRA (Branch Always) correctly implemented it now made sense to introduce BRZ (Branch on Zero) and BRP (Branch on Zero or Positive). These would be incredibly similar to BRA, but with an adding conditional statement. These instructions will jump to a memory location specified in a memory location, an immediate or using a location in a RegB when RegA’s contents match the expected condition.



As we can see, the only real change between BRA and BRZ is the inclusion of a single condition at the start of the micro-code. The only difference between BRZ and BRP was changing the condition here to instead end the instruction if the value is less than zero.

To allow the user to use registers effectively an instruction is needed that

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| MEM MODE | MEM  MODE | INSTRCT | INSTRCT | INSTRCT | INSTRCT | INSTRCT | INSTRCT |
| REGA | REGA | REGA | REGA | REGA | REGA | REGA | REGA |
| REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT | REGB OR MEM OR  DIRECT |
| MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT | MEM OR  DIRECT |

2 memory bits, followed by 6 bits of instruction identifier. Followed by 8 bit address of register A, then 8 bits of Reg B, or 16 bits of Memory Address or 16 bits

References

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| [1] | S. Heule, "How Many x86-64 Instructions Are There Anyway?," 7 March 2016. [Online]. Available: https://stefanheule.com/blog/how-many-x86-64-instructions-are-there-anyway/. |